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Emcore Corporation Attention: Daniel McGlynn 1600 Eubank Blvd. SE Albuquerque, NM 87123				
EXAMINER				
BARTON, JEFFREY THOMAS				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/773,343

**Applicant(s)**

SHARPS ET AL.

**Examiner**

Jeffrey T. Barton

**Art Unit**

1795

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 May 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 47.69, 112-126 and 128-133 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 47.69, 112-126, and 128-133 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Response to Amendment***

1. The amendment filed on 14 May 2009 does not place the application in condition for allowance.

***Status of Objections and Rejections Pending Since the  
Office Action of 27 February 2009***

2. All objections and rejections of claim 127 are obviated by cancellation of the claim.
3. The objection to claim 129 is withdrawn due to Applicant's amendment.
4. All rejections of claims 112-133 made under 35 U.S.C. §112, first and second paragraphs are withdrawn due to Applicant's amendment.
5. All other rejections are maintained.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 115, 117-120, 129, and 132 are rejected under 35 U.S.C. 102(e) as being anticipated by Boutros et al, U.S. Patent 6,635,507.

As seen in Figure 8, and with respect to independent claims 115 and 129, Boutros et al teaches a multijunction solar cell comprising a Ge substrate (802); a first region including the N and P GaAs layers (804) which form a first junction of the multijunction solar cell and the N and P GaInP layers (806) which form a second junction of the multijunction solar cell, wherein this first region includes the portion of said N and P GaAs layers (804) and the portion of the N and P GaInP layers (806) not directly below, but to the right of the GaAs cap layer. In a second region, the portions of corresponding N and P GaAs layers (804) and N and P GaInP layers (806) directly below the GaAs Cap support the bypass diode (810) to protect the cell against reverse biasing (see also col. 1, lines 16-22; and col. 7, lines 47-65). With respect to claims 115 and 129, these claims require that the top layer of the top cell has a first polarity and that the bottom layer of the bypass diode has the first polarity. In Figure 8, it is the Examiner's position that the GaAs N<sup>++</sup> layer can be considered to be the lower layer of the bypass diode, and thus, has the same polarity as the upper N-type GaInP layer of the upper solar cell. Indeed, as seen in Boutros et al's Figures 2A, 3A, and 4A, the bottom layer of the bypass diode (210, 310, 410) is N<sup>++</sup> and is the same polarity, i.e., N-type, as the top layer (208, 308, 408) of the solar cell. With respect to claims 115 and 129, when the GaAs P<sup>++</sup> layer is considered the lateral conduction layer (as per instant claims 118 and 132), then the bypass diode layers above it read on the instant etch stop layer. Alternatively, with respect to claim 119 and 129 when the GaAs Cap N<sup>++</sup> layer is

considered the lateral conduction layer, then the GaAs P<sup>++</sup> layer reads on the instant etch stop layer. Since both the GaAs P<sup>++</sup> and GaAs N<sup>++</sup> layers are highly doped, the structure also meets the limitations of claim 117.

With respect to claim 120, and as clearly seen in said Figure 8, the Ge substrate (802) forms an electrical connection path between the multijunction solar cell and the bypass diode.

In an alternative with respect to claim 129, the lower portion of the sequence of layers in the first region corresponds to N and P GaAs layers (804) and N and P GaInP layers (806), and the bypass diode (810) encompasses the upper portion of the sequence, located in the second region.

Since Boutros et al teaches the limitations of the instant claims, the reference is deemed to be anticipatory.

8. Claims 115-126 and 128-133 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho et al, WO 99/62125. In particular, see Figures 12 and 14B, and page 8, lines 16-23, which teach the claimed invention.

Regarding claim 115, Ho et al teaches a solar cell semiconductor device (Figure 14B) comprising: a substrate (1402); a sequence of layers (1404-1414) of material deposited on said substrate, including a first region (To left of trench 1438) in which the sequence of layers of material forms a plurality of cells of a multijunction solar cell, and a second region (Below and to the right of trench 1438) in which the sequence of layers corresponding to the sequence of layers forming said cells forms a support for a bypass

diode (e.g. tunnel diode layers to right of trench 1438) to protect said cell against reverse biasing; and a planar lateral conduction layer (1416) deposited over the sequence of layers in the second region for making electrical contact to an active region of said bypass diode; wherein the topmost layer of the topmost cell (1402) has a first polarity; and the bottom layer of the bypass diode (N++ tunnel diode layer 1420) has the same said first polarity as said topmost layer of said topmost cell; wherein the first region and the second region have an identical sequence of semiconductor layers (i.e. 1404-1414) where each layer in the first region has the same composition and thickness as the corresponding layer in the second region, subject to normal manufacturing variations, and the first region and the second region constitute an integral semiconductor body.

Regarding claim 116, Ho et al teaches a lateral conduction layer over the sequence of layers in the first region as claimed. (e.g. P++ tunnel diode layer 1418)

Regarding claim 117, layer 1418 is highly doped.

Regarding claim 118, P+ layer 1428 also reads on a highly doped lateral conduction layer, as is composed of GaAs.

Regarding claim 119, N++ tunnel diode layer 1420 reads on the instant etch stop layer.

Regarding claim 120, Ge substrate 1402 provides a conductive pathway between the solar cell and bypass diode. (Figure 14B)

Regarding claim 121, Ho et al teaches a metal layer (1440; alternatively 1442) disposed as claimed. Note that 1440 provides the instant shorting and connection functions in conjunction with 1442 and 1430

Regarding claim 122, Ho et al teaches a solar cell semiconductor device (Figure 14B) comprising: a substrate (1402); a sequence of layers (1404-1420) of semiconductor material deposited on said substrate including a first region (To left of trench 1438) in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell, and a second region (To right of trench 1438) in which a sequence of layers corresponding to the sequence of layers forming said at least one cell (1412-1420) forms a bypass diode that functions to protect said cell against reverse biasing; and wherein the sequence of layers in the first and second regions includes a lateral conduction layer (e.g. 1418) including a first portion disposed in said first region, and a second portion disposed in said second region and physically separated from said first portion; and further wherein: the topmost layer of the topmost cell (1402) has a first polarity; the bottom layer of the bypass diode (1420) has the same polarity as said first polarity of said topmost cell; and the first region and the second region have an identical sequence of semiconductor layers where each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region, subject to normal manufacturing variations, and form an integral semiconductor body.

Regarding claim 123, layer 1418 is a highly doped P++ layer.

Regarding claim 124, P+ layer 1414 also reads on a lateral conduction layer, and is composed of GaAs.

Regarding claim 125, window layer 1416 reads on a cap layer, with lateral conduction layer 1418 disposed directly over the cap layer.

Regarding claim 126, the second portion of layer 1418 makes electrical contact with layer 1420, which is a layer of the bypass diode.

Regarding claim 127, diode 1410 includes n and p GaAs layers disposed as claimed. (1412 and 1414)

Regarding claim 128, Ho et al teaches a metal layer (1440; alternatively 1442) disposed as claimed. Note that 1440 provides the instant shorting and connection functions in conjunction with 1442 and 1430

With respect to claim 129, in addition to the disclosure cited for claim 115 above, see Ho et al's Figure 12, where there is a cascade solar cell at a lower portion, a bypass diode (1214, 1216) at an upper portion, GaAs connecting layer (1210) which reads on the instant highly conductive lateral conduction layer, and layer (1222) which corresponds to the metal layer in instant claim 130 (see also page 7, line 16). The solar cell can be multijunction (see page 5, lines 15-23), and the semiconductor layers of the cascade solar cells can be p/n or n/p.

With respect to claims 131-133, layer 1210 meets the limitations of these claims.

Since Ho et al teaches the limitations of the instant claims, the reference is deemed to be anticipatory.



***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 121 and 130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boutros et al (U.S. Patent 6,635,507) as applied to claims 115, 117-120, 129, and 132 above, and further in view of Ho et al (WO 99/62125).

Boutros et al is relied upon for the reasons given above.

With respect to claims 121 and 130, Boutros et al does not specifically teach that said connecting contact (816) can be made from metal (i.e., instant metal layer).

However, as shown by reference sign (1436) in Figure 14B of Ho et al, it is well-known and conventional in the solar cell art to form connecting solar cell contacts from metal (see also page 8, lines 18-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have prepared Boutros et al's connecting contact (816) from metal because it is well-known and conventional in the art to do so, as shown by Ho et al.

### ***Double Patenting***

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 47, 69, 112-126, and 128-133 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-44 of U.S. Patent No. 7,115,811. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the '811 patent have the instant multijunction solar cell and bypass diode.

15. Claims 47, 69, 112-126, and 128-133 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 48-66, 68-80, and 82-98 of copending Application No. 10/723,456. Although the conflicting claims are not identical, they are not patentably distinct from each other because although not of the same scope as the instant claims, the claims of said copending application are anticipatory of the instant claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

16. Claims 47, 69, 112-126, and 128-133 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-12 of copending Application No. 11/247,828. Although the conflicting claims are not identical, they are not patentably distinct from each other because note in claim 2 of

said copending application wherein the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell and also forms the bypass diode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

17. Claims 47, 69, 112-126, and 128-133 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-19 of copending Application No. 11/280,379. Although the conflicting claims are not identical, they are not patentably distinct from each other because note in claim 2 of said copending application wherein the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell and also forms the bypass diode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

18. Claims 47, 69, and 112-126, and 128-133 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 15-20 of copending Application No. 11/614,332. Although the conflicting claims are not identical, they are not patentably distinct from each other because note in claim 16 of said copending application wherein the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell and also forms the bypass diode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

### ***Response to Arguments***

19. Applicant's arguments filed 14 May 2008 have been fully considered but they are not persuasive.

Regarding the rejections based on the Boutros et al reference, Applicant argues that the bottom layer of the bypass diode of Boutros et al is p-type. However, Applicant's arguments fail to persuade that the Examiner's position, namely that the N++ type cap layer 808 also reads on the bottom layer of the bypass diode, is improper. This position is not directly addressed in Applicant's remarks.

In arguments concerning claim 115, Applicant also misunderstands the Examiner's position as to the first region and second region of Boutros. The Examiner does not identify the first region as cell 804 and the second region as cell 806. The first region corresponds to the portions of cells 804 and 806 positioned not directly below, but to the right of layer 808 illustrated in Figure 8, while a second region includes the portions of the layers directly below layer 808. This is stated in the rejection as made above and in the previous office action. Clearly, the two regions include an identical sequence of layers as claimed, and the sequence of layers (804 and 806) forms a plurality of cells of a multijunction solar cell in the first region as claimed. This position was also stated in the rejection.

Regarding the Ho reference, Applicant's arguments are not persuasive. The Examiner agrees with Applicant that layers 1412-1420 of Ho correspond to the bypass diode 1410 of Ho et al. Applicant's statement that "The Office Action further equates the tunnel diode layers to the right of trench 1438 as the claimed bypass diode" is a misreading of the Office Action. In the text of the rejection, the tunnel diode layers are referenced as forming a support for the bypass diode. Accordingly the further arguments concerning this position being inconsistent with the understanding of one of ordinary skill in the art do not address the actual positions taken in the Office Action. As was clearly stated in the rejection, the bottom layer of the bypass diode is considered to be N++ layer 1420, while the topmost layer of the topmost cell is considered to be N-type Ge base/substrate 1402, as clearly stated in the rejection. Applicant asserts "With a proper interpretation of what actually is the bypass diode, Figure 14B plainly shows that layer 1412 is the bottom layer of the bypass diode". Applicant fails to provide any reason why layer 1420 cannot be considered the bottom layer. It is the Examiner's position that the Figure plainly shows that layer 1420 is the bottom layer of the diode. "Top" and "bottom" are terms defined relative to each other, but not specifically defined in the context of Figure 14B of Ho et al.

Applicant further appears to assert that layer 1402 cannot be the topmost layer of the topmost cell simply because "layer 1402 is a substrate". Clearly layer 1402 is indeed a substrate. It is not clear why Applicant believes that a substrate cannot be a layer of a cell. The claims are open to the interpretation given in the rejection, and the rejection is therefore clearly proper.

Applicant states that the double-patenting rejections will be addressed after indication of allowable subject matter in the present application. The Examiner points out that double patenting rejections are the only rejections currently applied to claims 47, 69, and 112-114.

It is noted that Applicant's remarks further state, "The Examiner's attention is directed to co-pending Application No. 11/058,595, and all pending prosecution and references cited in the prosecution history." The Examiner appreciates Applicant's concern, but notes that this is not a proper information disclosure statement. If Applicant wishes to cite any references or other portion of the prosecution history of this or any other related application, Applicant should submit the references on a properly formatted form PTO-1449.

### ***Conclusion***

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Jeffrey T. Barton whose telephone number is (571)272-1307. The examiner can normally be reached on M-F 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey T. Barton/  
Examiner, Art Unit 1795  
26 August 2009